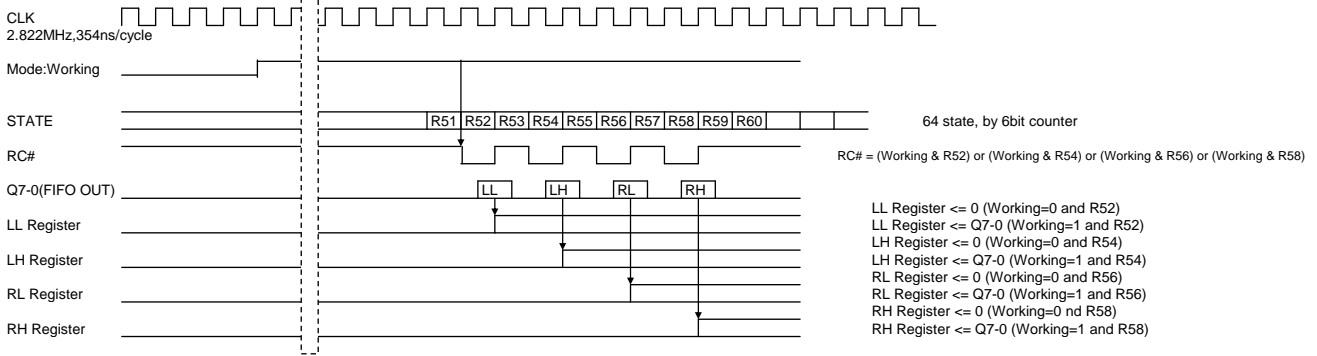
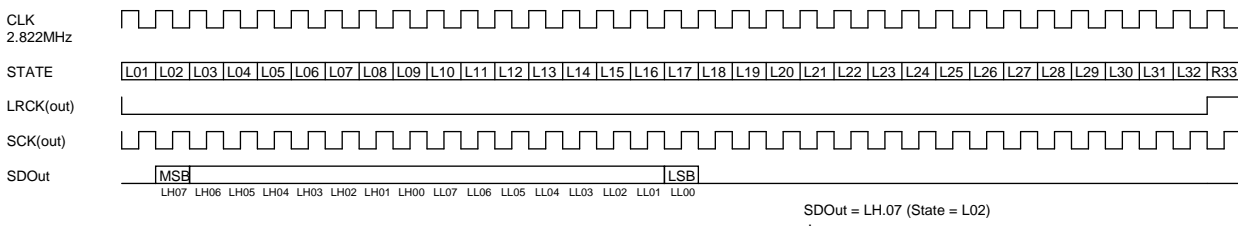


FIFO to I2S CPLD

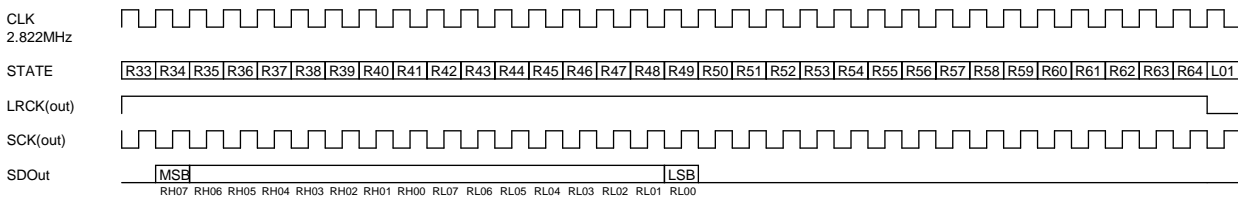
(1) FIFO to Register operation



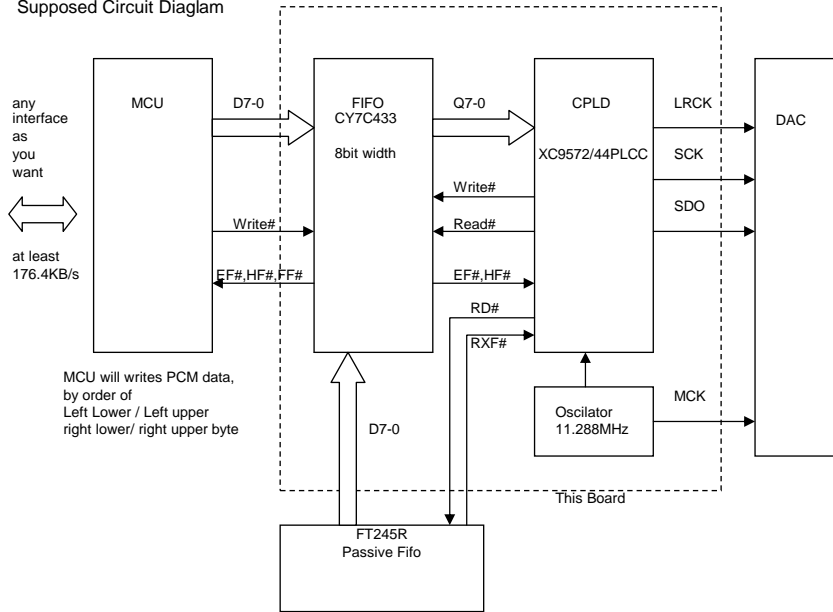
(2) Register to Output (Left)



(3) Register to Output (Right)

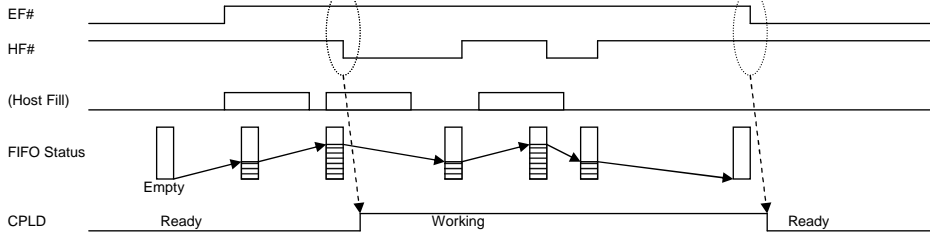


Supposed Circuit Diagram



FIFO Control

CPLD Mode control, for CY7C433 to CPLD



```

If (Working = 0)      --Ready Mode
  If (EF# = 1) and (HF# = 0)
    Working <= 1
  else
    Working <= Working
If (Working = 1)      --Working Mode
  If (EF# = 0)
    Working <= 0
  else
    Working <= Working
  
```

CPLD Read and Write Operation, for FT245R to CY7C433

